PCI SoundMAX™ Controller

AD1889

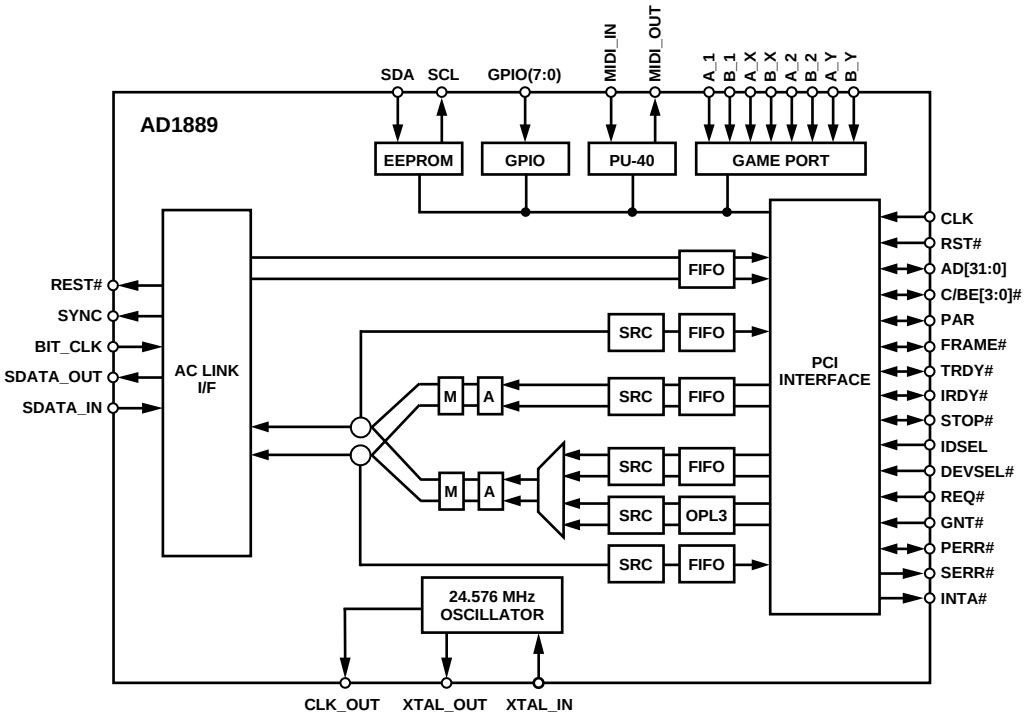
FEATURES

PCI Digital Controller (DC '97)
Supports Stereo Audio AC '97 Codecs
Full Duplex Capture and Playback Operation at Different Sample Rates
Sample Rates from 7 kHz to 48 kHz
WDM Accelerated Digital Mixing and Resampling
PCI Bus Master Interface
MS Direct Sound 3D Support
DOS Box Legacy Compatible
Compatible MIDI MPU-401 Port
OPL3 Compatible Music Synthesizer
ACPI Power Management Modes

PRODUCT OVERVIEW

The AD1889 PCI Digital Controller is an integral part of a PC 98 quality audio subsystem. targeted at Segment 0 PCs. In addition to audio legacy compatibility, the AD1889 provides a cost effective way to support simultaneous stereo audio, and host-based wavetable synthesis through the integration of an AC '97 2.0 compatible link and a PCI interface. The AD1889 drivers support Windows® 95, Windows 98, and DirectSound multimedia applications.

FUNCTIONAL BLOCK DIAGRAM



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REV. 0

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AD1889

FUNCTIONAL DESCRIPTION

The AD1889 is a full-duplex stereo digital controller that supports business audio and multimedia applications. The controller includes digital AC-Link converters, WDM digital mixing acceleration, and variable sample rate conversion.

Interface

The controller contains an PCI interface that handles up to two digital audio streams. The digital audio streams are sample rate converted and mixed to a common rate before being transmitted over the link to an AC '97 codec.

Sample Rates

The sample rates are completely independent for the incoming and outgoing .wav streams. The controller includes a variable sample rate converter, which allows instantaneous support for sample rates from 7 kHz to 48 kHz with a resolution of 1 Hz. The in-band integrated noise and distortion artifacts introduced by rate conversions are below –90 dB.

Digital Data Types

The codec can accept and generate mono and stereo 16-bit twos-complement PCM linear digital data, and 8-bit unsigned magnitude PCM linear data as specified in the control registers.

SoundBlaster Compatibility

SoundBlaster emulation in a Windows 95 and Windows 98 DOS Box is achieved through the combination of hardware digital mixing and software SoundBlaster trapping. SoundBlaster music may be host-generated wave table or internally generated music synthesis. Digital music is summed with the digital audio .wav stream prior to being sent to the AC-Link.

MIDI

The primary interface for communicating MIDI data to and from the host PC is the hardware MPU-401 interface. The MPU-401 interface includes a built-in 64-byte FIFO for communicating to the host bus.

Game Port

An IBM-compatible game port interface is provided on-chip. The game port supports up to two joysticks. Joystick registers supporting the Microsoft Direct Input standard for enhanced digital joysticks are included as part of the register map.

Power Down

The AD1889 supports the D0, D1, D2, and D3 power down states as detailed by the Audio Device Class Specification.

Digital Resampling

The AD1889 digitally resamples up to two streams of audio using the internal Sample Rate Converters (SRC). Streaming audio is rate converted to a common rate and then digitally mixed. The mixed stream may be sent back to the host (PCI bus) or sent to the AC '97 codec. When the AD1889 is sending data to the codec, all data is resampled to 48 kHz. During periods when the AC-Link is off, the AD1889 may be used to resample data to any rate from 7 kHz to 48 kHz in 1 Hz increments.

AC-Link

The AD1889 has an AC '97 2.0 compatible link for communication to an AC '97 codec like the AD1819, AD1881, or the AD1882. All streams are formatted by the AC-Link interface for communication with the codec. The two-chip system is capable of achieving greater than 90 dB SNR performance.

AD1889–SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25	°C
Digital Supply (V_{DD})	5.0	V

DIGITAL DECIMATION AND INTERPOLATION FILTERS*

Parameter	Min	Typ	Max	Units
Passband	0		$0.4 \times F_S$	Hz
Passband Ripple			±0.09	dB
Transition Band	$0.4 \times F_S$		$0.6 \times F_S$	Hz
Stopband	$0.6 \times F_S$		∞	Hz
Stopband Rejection	–74			dB
Group Delay			$12/F_S$	sec
Group Delay Variation Over Passband			0.0	µs

STATIC DIGITAL SPECIFICATIONS

Parameter	Min	Typ	Max	Units
High-Level Input Voltage (V_{IH}): Digtal Inputs	2			V
Low-Level Input Voltage (V_{IL})			9.8	V
High-Level Output Voltage (V_{OH}), I_{OH} = x mA	2.4			V
Low-Level Output Voltage (V_{OL}), I_{OL} = x mA	0.4			V
Input Leakage Current	–10		10	µA
Output Leakage Current	–10		10	µA

POWER SUPPLY

Parameter	Min	Typ	Max	Units
Power Supply Range—Digital	4.75		5.25	V
Power Supply Current		TBD		mA
Power Dissipation		TBD		mW
Digital Supply Current		55		mA

CLOCK SPECIFICATIONS*

Parameter	Min	Typ	Max	Units
Input Clock Frequency		24.576		MHz
Recommended Clock Duty Cycle	10	50	90	%

POWER-DOWN STATES

Parameter	Min	Typ	Max	Units
D0		82		mA
D2		38		mA
D3		12		mA

AD1889–SPECIFICATIONS

AC-LINK TIMING PARAMETERS (GUARANTEED OVER OPERATING TEMPERATURE RANGE)

Parameter	Symbol	Min	Typ	Max	Units
$\overline{\text{RESET}}$ Active Low Pulsewidth	t_{RST_LOW}	1.0			µs
$\overline{\text{RESET}}$ Inactive to BIT_CLK Start-Up Delay	$t_{RST2CLK}$	162.8			ns
SYNC Active High Pulsewidth	t_{SYNC_HIGH}		1.3		µs
SYNC Low Pulsewidth	t_{SYNC_LOW}		19.5		µs
SYNC Inactive to BIT_CLK Start-Up Delay	$t_{SYNC2CLK}$	162.8			ns
BIT_CLK Frequency			12.288		MHz
BIT_CLK Period	t_{CLK_PERIOD}		81.4		ns
BIT_CLK Output Jitter				750	ps
BIT_CLK High Pulsewidth	t_{CLK_HIGH}	32.56	40.7	48.84	ns
BIT_CLK Low Pulsewidth	t_{CLK_LOW}	32.56	40.7	48.84	ns
SYNC Frequency			48.0		kHz
SYNC Period	t_{SYNC_PERIOD}	20.8			µs
SYNC High Pulsewidth	t_{SYNC_HIGH}	0.00814	1.3		µs
Setup to Falling Edge of BIT_CLK	t_{SETUP}	15.0			ns
Hold from Falling Edge of BIT_CLK	t_{HOLD}	5.0			ns
BIT_CLK Rise Time	$t_{RISE\ CLK}$	2		6	ns
BIT_CLK Fall Time	$t_{FALL\ CLK}$	2		6	ns
SYNC Rise Time	$t_{RISE\ SYNC}$	2		6	ns
SYNC Fall Time	$t_{FALL\ SYNC}$	2		6	ns
SDATA_IN Rise Time	$t_{RISE\ CLKDIN}$	2		6	ns
SDATA_IN Fall Time	$t_{FALL\ DIN}$	2		6	ns
SDATA_OUT Rise Time	$t_{RISE\ DOUT}$	2		6	ns
SDATA_OUT Fall Time	$t_{FALL\ DOUT}$	2		6	ns
End of Slot 2 to BIT_CLK, SDATA_IN Low	t_{S2_PDOWN}			1.0	µs
Setup to Trailing Edge of RESET (Applies to SYNC, SDATA_OUT)	t_{OFF}	15			ns
Rising Edge of $\overline{\text{RESET}}$ to HI-Z Delay	t_{OFF}			25	ns

*Guaranteed, not tested.
Specifications subject to change without notice.

AC-Link Timing (TBA)

Figure 1. Cold Reset
Figure 2. Warm Reset
Figure 3. Clock Timing

PCI Bus Timing (TBA)

AD1889

ABSOLUTE MAXIMUM RATINGS*

Parameter	Min	Max	Units
Power Supplies			
Digital (DV_{DD})	–0.3	6.0	V
Input Current (Except Supply Pins)		±10.0	mA
Digital Input Voltage (Signal Pins)	–0.3	DV_{DD} + 0.3	V
Ambient Temperature (Operating)	0	+70	°C
Storage Temperature	–65	+150	°C

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1889JS	0°C to +70°C	100-Lead MQFP	S-100

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating

$T_{AMB} = T_{CASE} - (P_D \times \theta_{CA})$

T_{CASE} = Case Temperature in °C

P_D = Power Dissipation in W

θ_{CA} = Thermal Resistance (Case-to-Ambient)

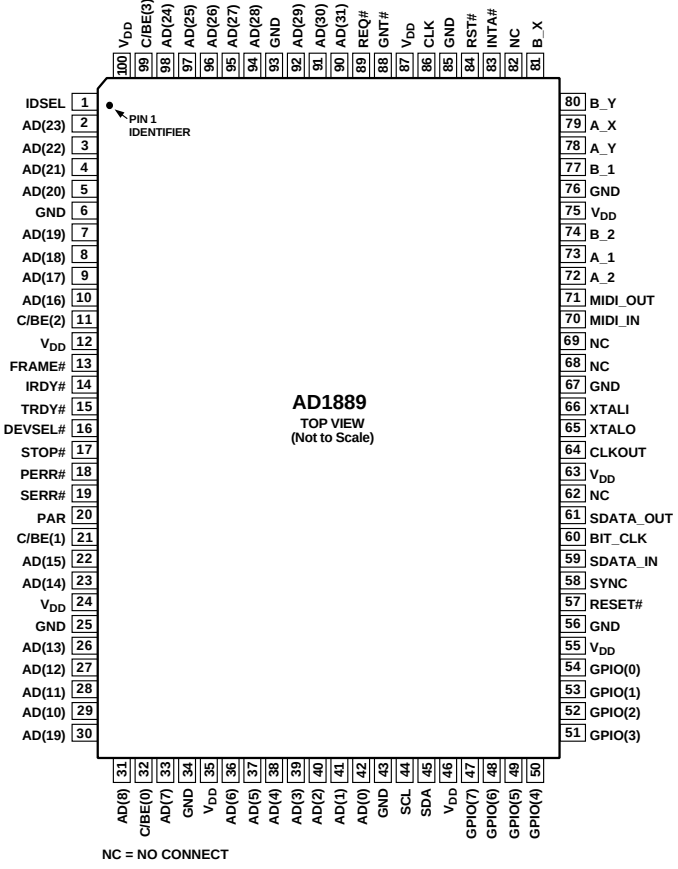
θ_{JA} = Thermal Resistance (Junction-to-Ambient)

θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
MQFP	91°C/W	?	?

PIN CONFIGURATION

100-Lead MQFP



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1889 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

PCI Bus Interface

Pin Name	MQFP	I/O	Description
CLK	86	I	Clock
$\overline{RST}$	84	I	PCI Reset
AD[31]	90	I/O	Address/Data Bus
AD[30]	91	I/O	Address/Data Bus
AD[29]	92	I/O	Address/Data Bus
AD[28]	94	I/O	Address/Data Bus
AD[27]	95	I/O	Address/Data Bus
AD[26]	96	I/O	Address/Data Bus
AD[25]	97	I/O	Address/Data Bus
AD[24]	98	I/O	Address/Data Bus
AD[23]	2	I/O	Address/Data Bus
AD[22]	3	I/O	Address/Data Bus
AD[21]	4	I/O	Address/Data Bus
AD[20]	5	I/O	Address/Data Bus
AD[19]	7	I/O	Address/Data Bus
AD[18]	8	I/O	Address/Data Bus
AD[17]	9	I/O	Address/Data Bus
AD[16]	10	I/O	Address/Data Bus
AD[15]	22	I/O	Address/Data Bus
AD[14]	23	I/O	Address/Data Bus
AD[13]	26	I/O	Address/Data Bus
AD[12]	27	I/O	Address/Data Bus
AD[11]	28	I/O	Address/Data Bus
AD[10]	29	I/O	Address/Data Bus
AD[9]	30	I/O	Address/Data Bus
AD[8]	31	I/O	Address/Data Bus
AD[7]	33	I/O	Address/Data Bus
AD[6]	36	I/O	Address/Data Bus
AD[5]	37	I/O	Address/Data Bus
AD[4]	38	I/O	Address/Data Bus
AD[3]	39	I/O	Address/Data Bus
AD[2]	40	I/O	Address/Data Bus
AD[1]	41	I/O	Address/Data Bus
AD[0]	42	I/O	Address/Data Bus
C/BE[3]	99	I/O	Command/Byte Enables
C/BE[2]	11	I/O	Command/Byte Enables
C/BE[1]	21	I/O	Command/Byte Enables
C/BE[0]	32	I/O	Command/Byte Enables
PAR	20	I/O	Parity
FRAME	13	I/O	Cycle Frame
RDY	15	I/O	Target Ready
IRDY	14	I/O	Initiator (Master) Ready
STOP	17	I/O	Stop
IDSEL	1	I	Initialization Device Select
DEVSEL	16	I/O	Device Select
REQ	89	O	Request
GNT	88	I	Grant
PERR	18	I/O	Parity Error
SERR	19	O	System Error
INTA	83	O	Interrupt A

EEPROM Interface

Pin Name	MQFP	I/O	Description
SCL	44	O	Clock
SDA	45	I	Serial Data

Game Port

Pin Name	MQFP	I/O	Description
A_1	73	I	Game Port A, Button #1
A_2	72	I	Game Port A, Button #2
A_X	79	I	Game Port A, X-Axis
A_Y	78	I	Game Port A, Y-Axis
B_1	77	I	Game Port B, Button #1
B_2	74	I	Game Port B, Button #2
B_X	81	I	Game Port B, X-Axis
B_Y	80	I	Game Port B, Y-Axis

MIDI Interface Signal

Pin Name	MQFP	I/O	Description
MIDI_IN	70	I	RXD MIDI Input
MIDI_OUT	71	O	TXD MIDI Output

AC-Link

Pin Name	MQFP	I/O	Description
BIT_CLK	60	I	Serial Port Serial Clock
SYNC	58	O	Serial Port Serial Data Frame Synchronization
SDATA_IN	59	I	Serial Port Serial Data Input
SDATA_OUT	61	O	Serial Port Serial Data Output
$\overline{RESET}$	57	O	Reset

Power Supplies

Pin Name	MQFP	I/O	Description
VDD	12, 24, 35, 46, 55, 63, 75, 87,100	I	Digital Supply Voltage (+5 V)
GND	6, 25, 34, 43, 56, 67, 76, 85, 93	I	Digital Ground

Miscellaneous

Pin Name	MQFP	I/O	Description
GPIO(7:0)	47, 48, 49, 50, 51,52, 53, 54	I/O	General Purpose I/O
CLKOUT	64	O	Clock Output
XTALI	66	I	Crystal/Clock Input
XTALO	65	O	Crystal/Clock Output
NC	62, 68, 69, 82		No Connect

PCI CONFIGURATION SPACE

Vendor ID **Address: 0x01–0x00**

Access: Read Only

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	8080h

VID[15:0] Vendor ID

Device ID **Address: 0x03– 0x02**

Access: Read Only

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0	8080h

DID[15:0] Device ID

Command **Address: 0x05–0x04**

Access: Read Only.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
CR15	CR14	CR13	CR12	CR11	CR10	FBTB	SEN	ADS	PER	VPS	MEN	SCEN	BMEN	MSEN	IOSEN	0000h

CR[15:0] Hardwired to 0. Reserved by PCI Rev. 2.1 Specification.

FBTB Fast Back-to-Back Enable. Controls master back-to-back transactions to different devices. Initialization software will set the bit if all targets are FBTB capable. Reset to 0.

0 = Fast back-to-back transactions are only allowed to the same agent (default).
1 = The master is allowed to generate fast back-to-back transactions to different agents.

SEN SERR# Enable.

0 = SERR# signal inactive.
1 = SERR# signal active.

ADS Address/Data Stepping. This bit indicates if the device is capable of address/data stepping.

PER Parity Error Response.

0 = No Parity error.
1 = Parity error detected.

VPS VGA Palette Snoop. This bit controls how VGA compatible and graphics devices handle accesses to VGA palette registers. This feature is unimplemented and hardwired to 0.

MEN Memory Write and Invalidate Enable. This feature is unimplemented and hardwired to 0.

SCEN Special Cycles Enable. Controls a device's action on Special Cycle operations. This bit is hard-wired to 0.

BMEN Bus Master Enable.

0 = Disables Bus Master Mode.
1 = Enables Bus Master Mode.

MSEN Memory Space Enable.

0 = Disabled.
1 = Enables response to memory space accesses.

IOSEN I/O Space Enable. This bit is hardwired to 0.

Status **Address: 0x07–0x06**

Access: Read Only

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
DPE	SSE	RMA	RTA	STA	DST1	DST0	DPED	FBTBC	UDFS	66MC	CL	SR3	SR2	SR1	SR0	0000h

DPE Detected Parity Error. This bit is set when a parity error is detected, even if parity error handling is disabled.

0 = No Parity Error.
1 = parity Error.

SSE Signaled System Error. This bit is set when the device asserts SERR#.

0 = SERR# deasserted.
1 = SERR# asserted.

RMA — Received Master Abort. This bit is set by a master device when a transaction is terminated with Master-Abort (except for Special Cycle).

0 = master transaction not terminated with Master-Abort.
1 = master transaction terminated with Master-Abort.

RTA — Received Target Abort. This bit is set by a target device whenever it terminates a transaction with Target-Abort.

0 = transaction not terminated with Target-Abort.
1 = transaction terminated with Target-Abort.

STA — Signaled Target Abort. This bit is set by a target device whenever it terminates a transaction with Target-Abort

0 = transaction not terminated with Target-Abort.
1 = transaction terminated with Target-Abort.

DST[1:0] — DEVSEL Timing. These bits encode the timing of DEVSEL#. These bits indicate the slowest time that a device asserts DEVSEL# for any bus command except Configuration Read and Configuration Write.

00 = Fast.
01 = Medium.
10 = Slow.
11 = reserved.

DPED — Data Parity Error Detect. This bit is set when three conditions are met 1) the bus agent asserted PERR# itself or observed PERR# asserted, 2) the agent setting the bit acted as the bus master for the operation in which the error occurred; or 3) the Parity Error Response bit is set.

0 = Data parity error did not occur.
1 = Data parity error did occur.

FBTBC — Fast Back-to-Back Capable. This bit indicates if the target is capable of accepting fast back-to-back transactions when the transactions are not to the same agent.

UDFS — UDF Support. This bit indicates that this device supports user-definable features. This bit is set when device specific configuration selections are presented to the user.

66MC — 66 MHz Capable. This bit indicates if the device is capable of running at 66 MHz.

0 = 33 MHz only.
1 = 66 MHz Capable.

CL — Capabilities List.

SR[3:0] — Reserved.

Class Code and Revision ID **Address: 0x0B–0x08**

Access: Read Only

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
CC23	CC22	CC21	CC20	CC19	CC18	CC17	CC16	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	0000h
CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0	

CC[23:0] — Class Code.

RID[7:0] — Revision ID.

Header Type and Latency Timer **Address: 0x0E–0x0D**

Access: Read Only

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
HT7	HT6	HT5	HT4	HT3	HT2	HT1	HT0	LT7	LT6	LT5	LT4	LT3	LT2	LT1	LT0	0000h

HT[7:0] — Header Type.

LT[7:0] — Latency Timer. This register specifies the value of the Latency Timer for the this bus mater (in unit of PCI bus clocks).

Base Address **Address: 0x13–0x10**
Access: Read Only

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
BA31	BA30	BA29	BA28	BA27	BA26	BA25	BA24	BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16	0000h
BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	

BA[31:0] Base Address. The AD1889 registers map into PCI memory space. The base register is 32 bits wide and mapping may be done anywhere in the 32-bit Memory Space. AD1889 register data is pre-fetchable. The AD1889 reserves 512 bytes in PCI Memory space for its register set.

Subsystem Vendor ID **Address: 0x2D–0x2C**
Access: Read Only

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
SVID15	SVID14	SVID13	SVID12	SVID11	SVID10	SVID9	SVID8	SVID7	SVID6	SVID5	SVID4	SVID3	SVID2	SVID1	SVID0	0000h

SVID[15:0] Subsystem Vendor ID.

Subsystem ID **Address: 0x2F–0x2E**
Access: Read

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
SID15	SID14	SID13	SID12	SID11	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	0000h

SID[15:0] Subsystem ID.

Capability Pointer **Address: 0x34**
Access: Read Only

D7	D6	D5	D4	D3	D2	D1	D0	Default
CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	0000h

CP[7:0] Capability Pointer. Pointer to first entry of capabilities list in configuration space.

Interrupt Line **Address: 0x3C**
Access: Read Only

D7	D6	D5	D4	D3	D2	D1	D0	Default
IL7	IL6	IL5	IL4	IL3	IL2	IL1	IL0	0000h

IL[7:0] Interrupt Line.

Interrupt Pin **Address: 0x3D**
Access: Read Only

D7	D6	D5	D4	D3	D2	D1	D0	Default
IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	0000h

IP[7:0] Interrupt Pin.

Min_Gn **Address: 0x3E**
Mnemonic:
Access: Read

D7	D6	D5	D4	D3	D2	D1	D0	Default
MG7	MG6	MG5	MG4	MG3	MG2	MG1	MG0	0000h

MG[7:0] Minimum GNT.

Max_Lat **Address: 0x3F**
Mnemonic:
Access: Read

D7	D6	D5	D4	D3	D2	D1	D0	Default
ML7	ML6	ML5	ML4	ML3	ML2	ML1	ML0	0000h

ML[7:0] Maximum Latency.

Capability ID **Address: 0xDC**
Access: Read

D7	D6	D5	D4	D3	D2	D1	D0	Default
CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0	0000h

CID[7:0] Capability ID.

Next Capability Pointer **Address: 0xDD**
Access: Read Only

D7	D6	D5	D4	D3	D2	D1	D0	Default
NCP7	NCP6	NCP5	NCP4	NCP3	NCP2	NCP1	NCP0	0000h

NCP[7:0] Next Capability Pointer.

Power Management Capabilities **Address: 0xDF–0xDE**
Access: Read Only

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	PMC9	PMC8	PMC7	PMC6	PMC5	PMC4	PMC3	PMC2	PMC1	PMC0	0000h

PMC[15:0] Power Management Capabilities

Power Management Control/Status **Address: 0XE1–0xE0**
Access: Read Only

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
PME_STAT	DSCALE1	DSCALE0	DSELECT3	DSELECT2	DESELECT1	DSELECT0	PME_EN	RES	RES	RES	RES	RES	RES	PSTATE1	PSTATE0	0000h

PME_STAT Power Management Event Status.
DSCALE[1:0] Data Scale.
DSELECT[3:0] Data Select.
PME_EN Power Management Event Enable.
PSTATE[1:0] Power State.

Power Management Bridge **Address: 0xE2**
Access: Read Only

D7	D6	D5	D4	D3	D2	D1	D0	Default
PMB7	PMB6	PMB5	PMB4	PMB3	PMB2	PMB1	PMB0	0000h

PMB[7:0] Power Management Bridge.

Power Management Data **Address: 0xE3**
Access: Read

D7	D6	D5	D4	D3	D2	D1	D0	Default
PMD7	PMD6	PMD5	PMD4	PMD3	PMD2	PMD1	PMD0	0000h

PMD[7:0] Power Management Data.

MEMORY SPACE REGISTER DEFINITION

DirectSound Register Space

Offset from Base Address 0

Address Range	Register Type	Base 0 Space Locations
0x000–0x03F	Mixer Control	64
0x040–0x0FF	PCI DMA Control	192
0x100–0x1FF	AC97 Codec Control	256
		512 Total

OPL-3 Compatible Music Synthesis Register Space

Offset from Base Address 1

Address Range	Register Type	Base 1 Space Locations
0x000	OPL-3 Music0: Address (W)/Status (R)	1
0x001	OPL-3 Music0: Data	1
0x002	OPL-3 Music1: Address (W)	1
0x003	OPL-3 Music1: Data	1
0x004–0x00F	Reserved	12
		16 Total

MIDI MPU-401 Register Space

Offset from Base Address 2

Address Range	Register Type	Base 2 Space Locations
0x000	MIDI Data (R/W)	1
0x001	MIDI UART: Status (R)/Command (W)	1
0x002–0x00F	Reserved	14
		16 Total

Legacy Control Register Space

Offset from Base Address 3

Address Range	Register Type	Base 3 Space Locations
0x000	Legacy Audio Control/Status	1
0x001–0x003	Reserved	3
0x004	Game Port RAW Data	1
0x005	Game Port Control/Status	1
0x006	Game Port Axis Data Low Byte	1
0x007	Game Port Axis Data High Byte	1
0x008–0x00F	Reserved	8
		16 Total

DirectSound Mixer Control Register Map

Address	Register
0x000–0x001	DMA Input Channels Wave/Synthesis Mixer Control
0x002–0x003	DMA Output Channels Resampler/ADC Mixer Control
0x004–0x005	DMA Input Channel Wave Attenuation
0x006–0x007	DMA Input Channel Synthesis Attenuation
0x008–0x009	Wave Channel Input Sample Rate
0x00A–0x00B	Resampler Channel Output Sample Rate
0x00C–0x00D	Chip Control/Status
0x00E–0x03F	(Reserved)

PCI DMA Control Register Map

Address	Register
0x040–0x043	RES Base Address/SGD Table Pointer
0X044–0x047	RES Current Address/SGD Current Pointer Address
0X048–0x04B	RES Base Count/SGD Pointer
0X04C–0x04F	RES Current Count
0x050–0x053	ADC Base Address/SGD Table Pointer
0x054–0x057	ADC Current Address/SGD Current Pointer Address
0x058–0x05B	ADC Base Count/SGD Pointer
0x05C–0x05F	ADC Current Count
0x060–0x063	SYNTH Base Address/SGD Table Pointer
0x064–0x067	SYNTH Current Address/SGD Current Pointer Address
0x068–0x06B	SYNTH Base Count/SGD Pointer
0x06C–0x06F	SYNTH Current Count
0x070–0x073	WAVE Base Address/SGD Table Pointer
0x074–0x077	WAVE Current Address/SGD Current Pointer Address
0x078–0x07B	WAVE Base Count/SGD Pointer
0x07C–0x07F	WAVE Current Count
0x080–0x082	RES Interrupt Current Count
0x083	(Reserved)
0x084–0x086	RES Interrupt Base Count
0x087	(Reserved)
0x088–0x08A	ADC Interrupt Current Count
0x08B	(Reserved)
0x08C–0x08E	ADC Interrupt Base Count
0x08F	(Reserved)
0x090–0x092	SYNTH Interrupt Current Count
0x093	(Reserved)
0x094–0x096	SYNTH Interrupt Base Count
0x097	(Reserved)
0x098–0x09A	WAVE Interrupt Current Count
0x09B	(Reserved)
0x09C–0x09E	WAVE Interrupt Base Count
0x09F	(Reserved)
0x0A0–0x0A3	RES PCI Control/Status
0x0A4–0x0A7	(Reserved)
0x0A8–0x0AB	ADC PCI Control/Status
0x0AC–0x0AF	(Reserved)
0x0B0–0x0B3	SYNTH PCI Control/Status
0x0B4–0x0B7	(Reserved)
0x0B8–0x0BB	WAVE PCI Control/Status
0x0BC–0x0BF	(Reserved)
0x0C0–0x0C3	PCI DMA Interrupt Status
0x0C4–0x0C7	PCI DMA Channel Stop Status
0x0C8–0x0C9	I/O Port Control
0x0CA–0x0CB	I/O Port Output Status
0x0CC–0x0CD	I/O Port Input Status
0x0CE–0xOFF	(Reserved)

AC97 Codec Control Register Map

Address Register	
0x100–0x101	Reset
0x102–0x103	Master Volume
0x104–0x105	(Reserved)
0x106–0x107	Master Volume Mono
0x108–0x109	(Reserved)
0x10A–0x10B	PC Beep Volume
0x10C–0x10D	Phone Volume
0x10E–0x10F	MIC Volume
0x110–0x111	LINE IN Volume
0x112–0x113	CD Volume
0x114–0x115	VIDEO Volume
0x116–0x117	AUX Volume
0x118–0x119	PCM OUT Volume
0x11A–0x11B	Record Select
0x11C–0x11D	Record Gain
0x11E–0x11F	(Reserved)
0x120–0x121	General Purpose
0x122–0x123	3D Control
0x124–0x125	(Reserved)
0x126–0x127	Powerdown Control/Status
0x128–0x173	Vendor Reserved
0x174–0x175	Serial Configuration
0x176–0x177	Miscellaneous Control
0x178–0x179	Sample Rate 0
0x17A–0x17B	Sample Rate 1
0x17C–0x17D	Vendor ID1
0x17E–0x17F	Vendor ID2
0x180–0x181	AC Link Interface Control/Status
0x182–0x1FF	(Reserved)

DIRECTSOUND MIXER CONTROL REGISTER DEFINITIONS

Wave/Synthesis Channel Mixer Control **Address: 0x000–0x001**

Mnemonic: WSMC
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RES	RES	WARQ1	WARQ0	RES	WAEN	WAST	WA16	RES	RES	SYRQ1	SYRQ0	RES	SYEN	RES	RES	0000h

WARQ[1:0] Wave Channel FIFO Request Point. Specifies the number of words empty in the Wave Channel FIFO when PCI transfer requests are generated.

00 = 4 mono words/2 stereo words (default).
01 = 12 mono words/6 stereo words.
10 = 18 mono words/9 stereo words.
11 = reserved.

WAEN Wave Channel Enable.

0 = Disable (Default).
1 = Enable.

WAST Wave Channel Mono/Stereo Select.

0 = Mono (Default).
1 = Stereo.

WA16 Wave Channel 8 bit/16 bit Select.

0 = 8-bit linear.
1 = 16-bit linear.

SYRQ[1:0] Synthesis Channel FIFO Request Point. Specifies the number of words empty in the Synthesis Channel FIFO when PCI transfer requests are generated.

00 = 4 mono words/2 stereo words (default).
01 = 12 mono words/6 stereo words.
10 = 18 mono words/9 stereo words.
11 = reserved.

SYEN Synthesis Channel Enable.

0 = Disable (Default).
1 = Enable.

Resampler/ADC Channel Mixer Control **Address: 0x002–0x003**
Mnemonic: RAMC
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RES	RES	RERQ1	RERQ0	RES	REEN	RES	RES	RES	RES	ACRQ1	ACRQ0	RES	ADEN	ADST	AD16	0000h

ERQ[1:0] Resampler Channel FIFO Request Point. Specifies the number of words of data available in the Resampler Channel FIFO when PCI transfer requests are generated.

00 = 4 mono words/2 stereo words (default).
01 = 12 mono words/6 stereo words.
10 = 18 mono words/9 stereo words.
11 = reserved.

REEN Resampler Channel Enable.

0 = Disable (Default).
1 = Enable.

ACRQ[1:0] ADC Channel FIFO Request Point. Specifies the number of words of data available in the ADC Channel FIFO when PCI transfer requests are generated.

00 = 4 mono words/2 stereo words (default).
01 = 12 mono words/6 stereo words.
10 = 18 mono words/9 stereo words.
11 = reserved.

ADEN ADC Channel Enable.

0 = Disable (Default).
1 = Enable.

ADST ADC Channel Mono/Stereo Select.

0 = Mono (Default).
1 = Stereo.

AD16 ADC Channel 8 bit/16 bit Select.

0 = 8 bit linear.
1 = 16 bit linear.

Wave Channel Digital Mix Attenuation **Address: 0x004–0x005**
Mnemonic: WADA
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
LWAM	RES	LWAA5	LWAA4	LWAA3	LWAA2	LWAA1	LWAA0	RWAM	RES	RWAA5	RWAA4	RWAA3	RWAA2	RWAA1	RWAA0	8080h

LWAM Left Wave Mix Mute.

0 = Unmute.
1 = Mute (Default).

LWAA[5:0] Left Wave Mix Attenuation. Least significant bit represents –1.5 dB.

00000 = 0.0 dB Attenuation. (Default).
11111 = –94.5 dB Attenuation.

RWAM Right Wave Mix Mute.

0 = Unmute.
1 = Mute (Default).

RWAA[5:0] Right Wave Mix Attenuation. Least significant bit represents –1.5 dB.

00000 = 0.0 dB Attenuation (Default).
11111 = –94.5 dB Attenuation.

Synthesis Channel Digital Mix Attenuation **Address: 0x006–0x007**
Mnemonic: SYDA
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
LSYM	RES	LSYA5	LSYA4	LSYA3	LSYA2	LSYA1	LSYA0	RSYM	RES	RSYA5	RSYA4	RSYA3	RSYA2	RSYA1	RSYA0	8080h

LSYM Left Synthesis Mix Mute.

0 = Unmute.
1 = Mute (Default).

LSYA[5:0] Left Synthesis Mix Attenuation. Least significant bit represents –1.5 dB.

00000 = 0.0 dB Attenuation (Default).
11111 = –94.5 dB Attenuation.

RSYM Right Synthesis Mix Mute.

0 = Unmute.
1 = Mute (Default).

RSYA[5:0] Right Synthesis Mix Attenuation. Least significant bit represents –1.5 dB.

00000 = 0.0 dB Attenuation (Default).
11111 = –94.5 dB Attenuation.

Wave Channel Sample Rate **Address: 0x008–0x009**
Mnemonic: WAS
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
WAS15	WAS14	WAS13	WAS12	WAS11	WAS10	WAS9	WAS8	WAS7	WAS6	WAS5	WAS4	WAS3	WAS2	WAS1	WAS0	BB80h

WAS[15:0] Wave Channel Sample Rate. Defines the conversion rate for the Wave channel. One LSB represents exactly one Hertz assuming a 24.576 MHz clock input on the XTALI pin. Usable range is 5,400 Hz (0x1518) to 48,000 Hz (0xBB80).

Resampler Channel Sample Rate **Address: 0x00A–0x00B**
Mnemonic: RES
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RES 15	RES 14	RES 13	RES 12	RES 11	RES 10	RES 9	RES 8	RES 7	RES 6	RES 5	RES 4	RES3	RES2	RES1	RES0	BB80h

RES[15:0] Resampler Channel Sample Rate. Defines the conversion rate for the Resampler channel. One LSB represents exactly one Hertz assuming a 24.576 MHz clock input on the XTALI pin. Usable range is 5,400 Hz (0x1518) to 48,000 Hz (0xBB80).

Chip Control/Status **Address: 0x00C–0x00D**
Mnemonic: CCS
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
CLKEN	RES	RES	RES	RES	PDALL	RES	XTD	RES	RES	RES	RES	WAU	SYU	REO	ADO	

CLKEN Clock out enable (24.576 MHz output clock).

0 = clock out disable (Default).
1 = clock out enable.

PDALL Power down entire chip.

0 = chip powered up (Default).
1 = chip powered down.

XTD XTAL Delay control.

0 = No wait (Default).
1 = Force wait of 4096 clock cycles before coming out of total power down.

WAU Wave Channel Underflow. This Read-Only Bit reports error status from the Wave channel. This bit is set high when the digital mixer requests Wave data and no new data is available. This is a sticky bit. It is reset when the Wave channel is disabled or when the part is reset.

SYU Synthesis Channel Underflow. This Read-Only Bit reports error status from the Synthesis channel. This bit is set high when the digital mixer requests Synthesis data and no new data is available. This is a sticky bit. It is reset when the Synthesis channel is disabled or when the part is reset.

REO Resampler Channel Overflow. This Read-Only Bit reports error status from the Resampler channel. This bit is set high when the digital resampler has new data to pass back to the host and the previous data has not been serviced. This is a sticky bit. It is reset when the Resampler channel is disabled or when the part is reset.

ADO ADC Channel Overflow. This Read-Only Bit reports error status from the ADC channel. This bit is set high when the AC link has new ADC record data and the previous data has not been serviced. This is a sticky bit. It is reset when the ADC channel is disabled or when the part is reset.

PCI DMA CONTROL REGISTER MAP (BASE 0)

DMA Channel Control/Status
Address: 0xA0–0xA3 RES

0xAB–0xA8 ADC

0xB3–0xB0 SYN

0xBB–0xB8 WAV
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RES	RES	RES	RES	RES	RES	RES	RES	EOL	SFLG	SGDS1	SGDS	IM1	IM0	LOOP	SGDE	

EOL — Scatter-Gather Descriptor (SGD) End Of Linked List (EOL).

0 = EOL bit not set in current SGD.
1 = EOL bit set in current SGD.

SFLG — Scatter-Gather Descriptor (SGD) Flag.

0 = Flag not set in current SGD.
1 = Flag set in current SGD.

SGDS[1:0] — Scatter-Gather Descriptor Status.

00 = Full Scatter-Gather Descriptor needed.
01 = Partial SGD Descriptor needed.
10 = SGD Valid.
11 = Reserved (Invalid status).

IM[1:0] — Interrupt Mode.

00 = Interrupt Disabled.
01 = Interrupt on Count.
10 = Interrupt on SGD Flag.
11 = Interrupt on End of Linked List (EOL).

LOOP — Loop Enable.

0 = Looping Disabled.
1 = Looping Enabled.

SGDE — Scatter-Gather Descriptor Mode Enable.

0 = Monolithic DMA Mode Enabled.
1 = Scatter-Gather DMA Mode Enabled.

Interrupt Current Count
Address: 0x80–0x82 RES

0x8A–0x88 ADC

0x92–0x90 SYN

0x9A–0x98 WAV
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RES	RES	RES	RES	RES	RES	RES	RES	ICC23	ICC22	ICC21	ICC20	ICC19	ICC18	ICC17	ICC16	
ICC15	ICC14	ICC13	ICC12	ICC11	ICC10	ICC9	ICC8	ICC7	ICC6	ICC5	ICC4	ICC3	ICC2	ICC1	ICC0	

ICC[23:0] — DMA Interrupt Current Byte Count. The value in this register counts down as data transfers take place on the PCI bus, tracking the number of bytes transferred. When the count reaches zero, and if Interrupt On Count is enabled, then an interrupt (INTA#) is generated on the PCI bus.

Interrupt Base Count
Address: 0x86–0x84 RES

0x8E–0x8C ADC

0x96–0x94 SYN

0x9E–0x9C WAV
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RES	RES	RES	RES	RES	RES	RES	RES	IBC23	IBC22	IBC21	IBC20	IBC19	IBC18	IBC17	IBC16	
IBC15	IBC14	IBC13	IBC12	IBC11	IBC10	IBC9	IBC8	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0	

IBC[23:0] DMA Interrupt Base Byte Count. The value in this register (minus possibly some off-alignment byte count) is automatically loaded into the Interrupt Current Count Register at the end of a PCI Master transaction, if the Interrupt Current Count has reached zero, and looping is enabled.

PCI DMA Interrupt
Address: 0xC3–0xC0
Mnemonic: DISR
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	PMAE	PTAE	
PTAI	PMAI	RES	RES	RES	RES	RES	RES	RES	SEPS	RES	RES	WAVI	SYNI	ADCI	RESI	

PMAE PCI Master Abort Interrupt Enable.

PTAE PCI Target Abort Interrupt Enable.

PTAI PCI Target Abort Interrupt This bit is set if a PCI Target Abort has taken place while AD1889 is transferring Master data, and if PTAE bit is set. Software can read this bit and must write a “1” to clear it.

PMAI PCI Master Abort Interrupt This bit is set if a PCI Master Abort has taken place while AD1889 is attempting a Master transaction, and if PMAE bit is set. Software can read this bit and must write a “1” to clear it.

SEPS Serial EEPROM Status. When this bit is high, it indicates that the serial EEPROM (if existent) has a checksum error. No interrupt is generated from this status. A “0” for this bit means that the serial EEPROM (if existent) has a valid checksum. This bit will not be set if no serial EEPROM is present. This bit can be cleared by writing a “1” to the bit location. Reset value is “0.”

WAVI WAV Channel Interrupt.

SYNI Synthesis Channel Interrupt.

ADCI ADC Channel Interrupt.

RESI Resampler Channel Interrupt.

DMA Channel Stop Status **Address: 0xC7–0xC4**
Mnemonic: CHSS
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	
RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	WAVS	SYNS	ADCS	RESS	

Note: These bits will be set if the corresponding channel, while attempting a PCI Master transaction, encounters either a Target Abort or a Master Abort to terminate the transaction. Another way that these bits can be set is if the corresponding channel has reached the end of its DMA buffer and looping is not enabled. The channel will be stopped until software re-enables the channel by writing a "1" to the corresponding bit in this register to clear it.

WAVS WAV Channel Stopped.

SYNS Synthesis Channel Stopped.

ADCS ADC Channel Stopped.

RESS Resampler Channel Stopped.

GPIO Port Control **Address: 0xC9–0xC8.**
Mnemonic: IPC
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RES	RES	RES	RES	RES	RES	RES	RES	IPC7	IPC6	IPC5	IPC4	IPC3	IPC2	IPC1	IPC0	0x00FF

IPCn GPIO Port Control.

0 = Output.
1 = Input (Default).

GPIO Output Port Status **Address: 0xCB–0xCA**
Mnemonic: OP
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RES	RES	RES	RES	RES	RES	RES	RES	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	

OP[7:0] GPIO Output Port Status.

0 = Output low.
1 = Output high.

GPIO Input Port Status **Address: 0xCD–0xCC**
Mnemonic: IP
Access: Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
RES	RES	RES	RES	RES	RES	RES	RES	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0	

IP[7:0] GPIO Input Port Status.

0 = Input low.
1 = Input high.

AC97 CODEC CONTROL REGISTER MAP (BASE 0)

AC Link Interface Control/Status Address: 0x181-0x180
Mnemonic: ACIC
Access: Read Only and Read/Write

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
ACRDY	RES	RES	RES	RES	RES	FSYH	FSDH	res	RES	RES	RES	VSRM	ASOE	ACRD	ACIE	0x0000

ACRDY Analog Codec Ready Status (Read only).

FSYH Force Sync High.

FSDH Force SDATA_OUT High.

VSRM Variable Sample Rate Mode.

ASOE Audio Stream Output Enable.

ACRD Analog Codec Reset Disable.

ACIE Analog Codec Interface Enable.

MIDI MPU-401 REGISTER SPACE (BASE 2)

MIDI Data **Address: 0x00**
Mnemonic: MIDA
Access: Read Only and Read/Write

D7	D6	D5	D4	D3	D2	D1	D0	Default
MIDA7	MIDA6	MIDA5	MIDA4	MIDA3	MIDA2	MIDA1	MIDA0	0x00

MIDA[7:0] MIDI Data.

MIDI Status/Command **Address: 0x01**
Mnemonic: MISC
Access: Read/Write

D7	D6	D5	D4	D3	D2	D1	D0	Default
DRR	DSR	RES	RES	RES	RES	RES	RES	ox80
CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	0x80

DRR (R) Data Receive Ready. When read, this bit indicates that you can (0) or cannot (1) read from the MIDI Data Register. (Unreadable = 1, Readable = 0).

DSR (R) Data Send Ready. When read, this bit indicates that you can (0) or cannot (1) write to the MIDI Data Register. (Full = 1, Empty = 0).

CMD[7:0] (W) MIDI command. Write MPU-401 commands to bits [7:0] of this register.

LEGACY CONTROL REGISTER SPACE (BASE 3)

Legacy Audio Control/Status **Address: 0x00**
Mnemonic: LCS
Access: Read Only and Read/Write

D7	D6	D5	D4	D3	D2	D1	D0	Default
MI	RES	GI	GIE	RES	RES	SSIW	MIE	0x00

MIE MIDI Interrupt Enable.

SSIW Subsystem ID Write Enable.

GIE Gameport Interrupt Enable.

GI(RO) Gameport Interrupt Pending.

MI(RO) MIDI Interrupt Pending.

Joystick RAW Data **Address: 0x04**
Mnemonic: JRD
Access: Read Only

D7	D6	D5	D4	D3	D2	D1	D0	Default
JOY7	JOY6	JOY5	JOY4	JOY3	JOY2	JOY1	JOY0	0xF0

JOY[7:0] Joystick RAW Data.

Joystick Control/Status **Address: 0x05**
Mnemonic: JCS
Access: Read/Write

D7	D6	D5	D4	D3	D2	D1	D0	Default
JRDY	JWRP	JSEL1	JSEL0	JMSK3	JMSK2	JSMK1	JMSK0	(0xF0

JMSK[3:0] Joystick Axis Mask. JRDY bit calculated on axes selected by JMSK only.

(RW) xxx1 = Enable AX.
xx1x = Enable AY.
x1xx = Enable BX.
1xxx = Enable BY.

JSEL[1:0] Joystick Select.

(RW) 00 = Read AX (16 bits) from (Base3 + 06) and (Base3 + 07).
01 = Read AY (16 bits) from (Base3 + 06) and (Base3 + 07).
10 = Read BX (16 bits) from (Base3 + 06) and (Base3 + 07).
11 = Read BY (16 bits) from (Base3 + 06) and (Base3 + 07).

JWRP (RW) Joystick Wrap Mode. Continuous joystick sampling mode - ~ every 16 ms.

JRDY (RO) Joystick Ready. Sampling complete, joystick data ready for reading.

Joystick Axis Low Byte **Address: 0x06**
Mnemonic: JALB
Access: Read/Write

D7	D6	D5	D4	D3	D2	D1	D0	Default
JAX7	JAX6	JAX5	JAX4	JAX3	JAX2	JAX1	JAX0	0xFF

JAX[7:0] Joystick Axis Low Byte. Axis to be read is selected by the JSEL bits in the Joystick Control/Status register. A write to this register starts a sampling cycle.

Joystick Axis High Byte **Address: 0x07**
Mnemonic: JALB
Access: Read/Write

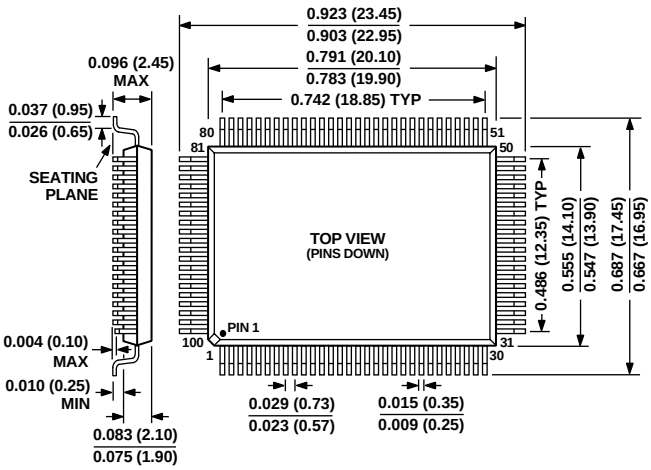
D7	D6	D5	D4	D3	D2	D1	D0	Default
JAX15	JAX14	JAX13	JAX12	JAX11	JAX10	JAX9	JAX8	0xFF

JAX[15:8] Joystick Axis High Byte. Axis to be read is selected by the JSEL bits in the Joystick Control/Status register. A write to this register starts a sampling cycle.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

100-Lead MQFP
(S-100)



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