

# Configurability of the PA 7300LC

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Rather than choosing a single, inflexible memory and level-2 cache configuration, we architected the PA 7300LC so that system designers can make price and performance trade-offs themselves. Most of the choices available to designers are in the memory system.

## Bus Frequencies

The PA 7300LC GSC (general system connect) bus interface supports several CPU:GSC frequency ratios. GSC frequencies at or near the bus maximum frequency of 40 MHz can be maintained even when the CPU is running at noninteger multiples of the bus frequency (e.g., 132 MHz).

## Memory Interface

The memory interface can be designed with either 64-bit or 128-bit (72-bit or 144-bit with error correction) data paths. A maximum of 16 memory banks is supported, and each bank can hold from 8M bytes to 512M bytes of DRAM. The DRAM technology can be either FPM (fast page mode) or EDO (extended data out), with chip sizes from 4M bits to 256M bits. A broad range of DRAM speeds is allowed, as DRAM timing can be software programmed using a nine-element MIOC (memory and I/O controller) timing vector.

Memory error correction is optional. Single-bit correct and double-bit and four-bit burst error detection schemes are available, all with sufficient error logging for system diagnosis and program data protection.

## Level-2 Cache

The level-2 cache is completely optional. Three types of SRAM are supported: register-to-register, flow-through, and asynchronous. Depending on the SRAM speed and CPU frequency, level-2 cache latencies of two, three, or four CPU cycles can be programmed into the MIOC. Parity error protection on the SRAM data is also optional.

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